IN THE CLAIMS

Please cancel claim 1 and add the following claims:

1. (Canceled.)

2-34. (Previously Canceled.)

35. (New.) A method of operation of an integrated circuit memory device comprising:

receiving a command that specifies a calibration mode;

while in the calibration mode, calibrating a voltage swing level to produce a calibrated voltage swing level, wherein calibrating includes:

driving a signal having an amount of voltage swing onto a first signal line to produce a voltage level; and

adjusting the amount of voltage swing of the signal based on a comparison between a reference voltage level and the voltage level produced by driving the signal; and

exiting the calibration mode, wherein, upon exiting the calibration mode, the integrated circuit memory device is operable to drive data onto the first signal line in accordance with the calibrated voltage swing level.

36. (New.) The method of claim 35, wherein calibrating is performed concurrently with a memory refresh operation.

37. (New.) The method of claim 35, wherein the command that specifies the calibration mode is a register read command.

38. (New.) The method of claim 35, wherein calibrating is performed during initialization of the integrated circuit memory device, and wherein the method further comprises periodically updating the calibrated voltage swing level after initialization.

39. (New.) The method of claim 35, further including:

actively coupling a comparator to the first signal line during the calibration mode;

when the comparator is coupled to the first signal line, calibrating the voltage swing level by using the comparator to compare the voltage level produced by driving the signal onto the first signal line with the reference voltage level; and

actively isolating the comparator from the first signal line upon exiting the calibration mode.

40. (New.) The method of claim 35, further including receiving the reference voltage level from a source external to the integrated circuit memory device.

41. (New.) The method of claim 35, further including generating the reference voltage level using a reference voltage generator disposed internally within the integrated circuit memory device.

42. (New.) The method of claim 35, wherein the amount of voltage swing is represented by a code held in a counter, wherein adjusting the amount of voltage swing further comprises updating the code.

43. (New.) The method of claim 42, wherein adjusting the amount of voltage swing includes activating a number of output driver transistors based on the code.

44. (New.) The method of claim 35, wherein the voltage level that is derived from the amount of voltage swing is derived by dividing between a predetermined voltage level and a voltage swing potential corresponding to the amount of voltage swing generated when the signal is driven onto the first signal line.

45. (New.) A method of operation of an integrated circuit memory device, the method comprising:

during a memory refresh period, calibrating a voltage swing characteristic of an output driver of the integrated circuit memory device, wherein calibrating includes:

driving a signal onto an external signaling path; and

adjusting an amount of voltage swing of the output driver based on a comparison between a reference voltage level and a voltage level produced by driving the signal.

46. (New.) The method of claim 45, wherein adjusting the amount of voltage swing of the output driver includes:

adjusting the amount of voltage swing in a first direction when the voltage level exceeds the reference voltage level; and

adjusting the amount of voltage swing in a second direction when the reference voltage level exceeds the voltage level.

47. (New.) The method of claim 45, wherein the voltage swing characteristic of the output driver is calibrated periodically.

48. (New.) The method of claim 45, further including receiving a command that instructs the integrated circuit memory device to calibrate the voltage swing characteristic.

49. (New.) The method of claim 45, wherein adjusting the amount of voltage swing further includes:

actively coupling a comparator to a signal line of the signaling path;

comparing the voltage level with the reference voltage level using the comparator coupled to the signal line; and

actively isolating the comparator from the signal line upon exiting the calibration mode.

50. (New.) The method of claim 49, wherein adjusting the amount of voltage swing further includes deriving the voltage level by dividing between a predetermined voltage level and a voltage swing potential produced by driving the signal.

51. (New.) The method of claim 45, further including receiving the reference voltage level.

52. (New.) The method of claim 45, further including generating the reference voltage level within the integrated circuit memory device.

53. (New.) The method of claim 45, further including storing a digital value in a register, wherein the digital value represents the amount of voltage swing of the output driver.

54. (New.) An integrated circuit memory device that is operable to calibrate a driver output voltage swing characteristic during a memory refresh period, the integrated circuit memory device comprising:

a first output driver to drive a signal onto a first external signal line; and

an adjustment circuit, coupled to the first output driver, to adjust an amount of voltage swing of the first output driver based on a comparison between a reference voltage level and a voltage level produced by driving the signal.

55. (New.) The integrated circuit memory device of claim 54, wherein:

the amount of voltage swing is adjusted in a first direction when the voltage level exceeds the reference voltage level; and

the amount of voltage swing is adjusted in a second direction when the reference voltage level exceeds the voltage level.

56. (New.) The integrated circuit memory device of claim 54, wherein the adjustment circuit includes a comparator to compare the reference voltage level and the voltage level produced by driving the signal.

57. (New.) The integrated circuit memory device of claim 56, further including a reference voltage generator, coupled to the comparator, to generate the reference voltage level.

58. (New.) The integrated circuit memory device of claim 54, wherein the reference voltage level is received from a source external to the integrated circuit memory device.

59. (New.) The integrated circuit memory device of claim 54, further including a voltage divider coupled to the first external signal line and the first output driver, to produce the voltage level based on the amount of voltage swing generated, wherein the voltage level is determined based on a ratio of resistors of the voltage divider.

60. (New.) The integrated circuit memory device of claim 59, further including a second output driver coupled to a second external signal line, wherein the voltage divider includes a first end and a second end, wherein the first end is coupled to the first external signal line and the second end is coupled to the second external signal line.

61. (New.) The integrated circuit memory device of claim 54, further comprising a counter coupled to the adjustment circuit and the first output driver, wherein the amount of voltage swing is determined by a code held in the counter, wherein the code is adjusted based on the comparison between the reference voltage level and the voltage level produced by driving the signal.

62. (New.) The integrated circuit memory device of claim 61, wherein the first output driver includes a plurality of transistors, wherein the signal is driven onto the first external signal line by activating a number of transistors of the plurality of transistors, wherein the number of transistors activated is determined by the code.

63. (New.) The integrated circuit memory device of claim 54, wherein the first output driver includes a plurality of transistors, wherein the amount of voltage swing of the first output driver is determined by a number of transistors of the plurality of transistors activated.

64. (New.) A memory device that is operable to calibrate an amount of voltage swing of a driver means, wherein the memory device is a dynamic random access memory device, the memory device comprising:

driver means for driving a signal onto an external signal line;

adjustment means to adjust the amount of voltage swing of the driver means, wherein the amount of voltage swing is adjusted based on a comparison between a reference voltage level and a voltage level produced by driving the signal; and

isolation means coupled to the driver means and adjustment means, the isolation means for isolating the adjustment means from the driver means such that the driver means is operable for driving data onto the external signal line in normal operation after the amount of voltage swing of the driver means has been calibrated.

65. (New.) The memory device of claim 64, wherein the adjustment means includes:

means for comparing the voltage level produced by driving the signal and the reference voltage level;

voltage dividing means to produce the voltage level based on the amount of voltage swing of the driver means; and

counting means for storing a code representative of the amount of voltage swing, wherein the code is adjusted in response to the comparison between the voltage level and the reference voltage.

66. (New.) The memory device of claim 64, wherein the amount of voltage swing of the driver means is calibrated concurrently with a memory refresh operation.

67. (New.) The memory device of claim 64, wherein the amount of voltage swing of the driver means is calibrated periodically.

68. (New.) A memory device that is operable to calibrate an amount of voltage swing, wherein the memory device is a dynamic random access memory device, the memory device comprising:

a driver circuit to drive a signal onto an external signal line;

an adjustment circuit to adjust an amount of voltage swing of the driver circuit based on a comparison between a reference voltage level and a voltage level produced by the driver circuit driving the signal; and

an isolation circuit coupled to the driver circuit and the adjustment circuit, the isolation circuit to isolate the adjustment circuit from the driver circuit such that the driver circuit is operable to drive data onto the external signal line after the amount of voltage swing of the driver circuit has been calibrated.

69. (New.) The memory device of claim 68, wherein the driver circuit includes a transistor having an effective width that is configured to adjust the amount of voltage swing of the output driver.

70. (New.) The memory device of claim 69, wherein the amount of voltage swing is represented by a code held in a counter and wherein the width of the transistor is configured based on the code, and wherein the code is adjusted based on the comparison between the reference voltage level and the voltage level derived from driving the signal.

71. (New.) The memory device of claim 68, wherein the amount of voltage swing is calibrated during a memory refresh operation.

72. (New.) The memory device of claim 68, wherein the driver circuit includes a first output driver and a second output driver, wherein the first output driver is coupled to the first external signal line and the second output driver is coupled to a second external signal line, and wherein the adjustment circuit includes a voltage divider coupled to the first and second external signal lines, wherein the voltage level produced by the driver circuit driving the signal is based on a ratio of resistors of the voltage divider.

73. (New.) The memory device of claim 68, wherein the adjustment circuit includes a comparator to compare the reference voltage level and the voltage level produced by driving the signal.

74. (New.) The memory device of claim 68, wherein:

the amount of voltage swing is adjusted in a first direction when the voltage level exceeds the reference voltage level; and

the amount of voltage swing is adjusted in a second direction when the reference voltage level exceeds the voltage level.

75. (New.) The memory device of claim 68, further including a reference voltage generator, coupled to the comparator, to generate the reference voltage level.

76. (New.) The memory device of claim 68, wherein the isolation circuit includes a passgate that actively couples the adjustment circuit to the driver circuit in response to a command that specifies that the amount of voltage swing is to be calibrated.